

**Amendments to the Claims:**

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A ferroelectric memory, comprising:

a microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the microstructure;

a substrate, the microstructure being centrally positioned and integrated on the substrate; and

a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

2. (Currently Amended) A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being peripherally positioned and integrated on the substrate, wherein the passive matrix array is electrically connected to the line driver circuit.

3. (Currently Amended) A ferroelectric memory, comprising:
  - a first microstructure;
  - a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the first microstructure;
  - a second microstructure;
  - a peripheral circuit comprising a line driver circuit for the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and
  - a substrate, the first and second microstructures being integrated on the substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

4. (Currently Amended) The ferroelectric memory according to claim 1, further including a plurality of microstructures integrated on the substrate, the passive matrix array being formed on each of the plurality of microstructures.

5. (Previously Presented) The ferroelectric memory according to claim 1, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

6. (Previously Presented) The ferroelectric memory according to claim 5, wherein the substrate is formed by transfer-molding a photocurable resin.

7. (Withdrawn) A ferroelectric memory, comprising:
  - a first microstructure;

a plurality of pairs of a passive matrix array that each includes memory cells formed of ferroelectric capacitors, the plurality of pairs of the passive matrix array being provided on the first microstructure;

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and

a substrate, at least one of the pairs of the passive matrix array being provided on each side of the substrate.

8. (Currently Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors; capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array,

a peripheral circuit comprising a line driver circuit for the passive matrix array; an associated circuit having a same or a different function as the memory cells; a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate, wherein the line driver circuit is positioned and electrically connected with the passive matrix array.

9. (Currently Amended) A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors; capacitor, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array,

a peripheral circuit comprising a line driver for the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated, positioned and integrated on the single microstructure, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

10. (Currently Amended) A ferroelectric memory, comprising:

a first microstructure;  
a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a central part of the second microstructure to be integrated; and

a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the peripheral circuit being separately formed on the second microstructure, wherein the line driver circuit is electrically connected with the passive matrix array.

11. (Withdrawn) A ferroelectric memory, comprising:

a plurality of microstructures;  
a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on each of the plurality of microstructures;  
a peripheral circuit for the passive matrix array; and  
a substrate, the microstructures being provided in layers to be integrated in the substrate.

12. (Currently Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a

ferroelectric capacitor being defined by an intersection of row and column electrodes  
sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit  
comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a microstructure;  
separately forming the peripheral circuit on a substrate; and  
centrally positioning and integrating the microstructure on the substrate,

wherein the passive matrix array is electrically connected to the line driver circuit.

13. (Currently Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes  
sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit  
comprising a line driver circuit peripheral to the passive matrix array, the method comprising:  
forming the passive matrix array centrally disposed on a substrate;  
separately forming the peripheral circuit on a microstructure; and  
integrating the microstructure on the substrate, wherein the line driver circuit  
is peripherally positioned and electrically connected with the passive matrix array.

14. (Currently Amended) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes  
sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit  
comprising a line driver circuit peripheral to the passive matrix array, the method comprising:  
forming the passive matrix array on a first microstructure;  
separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate, wherein the line driver circuit is peripherally positioned and electrically connected with the passive matrix array.

15. (Previously Presented) The method of fabricating a ferroelectric memory according to claim 12, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

16. (Previously Presented) The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the step of providing the microstructure includes providing a fluid which contains the microstructure to a surface of the substrate.

17. (Withdrawn) A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming a plurality of pairs of the passive matrix array on a first microstructure;

forming the peripheral circuit on a second microstructure; and  
introducing at least one of the pairs on each side of a substrate.

18. (Currently Amended) A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;  
separately forming the peripheral circuit on a second microstructure which is  
larger than the first microstructure; and  
providing the first microstructure in a central part of the second microstructure  
to be integrated, wherein the line driver circuit is electrically connected with the passive  
matrix array.

19. (Currently Amended) A method of fabricating a ferroelectric memory, which  
includes a passive matrix array including memory cells formed of ferroelectric capacitors, a  
ferroelectric capacitor being defined by an intersection of row and column electrodes  
sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit  
comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of  
microstructures; and

providing the microstructures in layers to be integrated in a substrate, wherein  
the passive matrix array on each of the plurality of microstructures is electrically connected to  
a respective drain wiring.

20. (Currently Amended) The ferroelectric memory according to claim 2, further  
including a plurality of microstructures integrated on the substrate, at least one of word line  
driver circuit and bit line driver circuit being formed on each of the plurality of  
microstructures.

21. (Previously Presented) The ferroelectric memory according to claim 2,  
wherein:

a recess portion in which the microstructure is provided is formed in the  
substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

22. (Currently Amended) The ferroelectric memory according to claim 3, further including a plurality of microstructures integrated on the substrate, the passive matrix array and at least one of word line driver circuit and bit line driver circuit being formed on each of the plurality of microstructures.

23. (Previously Presented) The ferroelectric memory according to claim 3, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

24. (Previously Presented) The method of fabricating a ferroelectric memory according to claim 13, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

25. (Previously Presented) The method of fabricating a ferroelectric memory according to claim 14, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

**Amendments to the Drawings:**

The attached replacement drawing sheets make changes to Figs.. 24-26C and replaces the original sheets with Figs. 24-26C.

Attachment: Replacement Sheets